AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended): An analogue-to-digital converter having differential inputs and a parallel structure, comprising at least one network of N series resistors with value r and one network of N comparators wherein:

the series resistor network receives a reference voltage and is traversed by a fixed current I_0;

the row i, i varying from 1 to N, comparator includes:

a dual differential amplifier with four inputs, two inputs receiving a differential voltage to be converted, a third input being connected to a row i resistor of the network, and a fourth input being connected to an N-i row resistor of the network, the dual differential amplifier supplying a voltage representing a difference of the form (VS-VSN) - (N-2i)r.I_0, and the comparator switching in one direction or the other depending on the level of the voltage and on the row i of the comparator when said difference changes sign,

wherein the resistor network is supplied by a variable reference voltage originating from a servoloop circuit which locks the voltage level of the middle of the resistor network at a voltage equal to the common mode voltage (VS-VSN)/2 of the differential voltage to be converted,

wherein the dual differential amplifier with four inputs is composed of two single differential amplifiers, the outputs of which are connected in parallel, each of them receiving, on the one hand, one of the two input differential voltages and, on the other hand, one of the two voltages originating from the resistor network.

2. (Previously Presented): The converter as claimed in claim 1, wherein the servoloop circuit supplies a variable reference voltage to the resistor network and to another resistor network similar to the first, locking being performed starting from a voltage taken from the middle of the other resistor network.

3. (Cancelled).

4. (Previously Presented): The converter as claimed in claim 2, wherein the dual differential amplifier with four inputs is composed of two single differential amplifiers, the outputs of which are connected in parallel, each of them receiving, on the one hand, one of the two input differential voltages and, on the other hand, one of the two voltages originating from the resistor network.